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Further aspects of damage-induced junction mechanisms and the role of phosphorus movement in double-layer in-chamber annealed In–Sn/ITO/InP solar cells

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Abstract. The research effort dedicated to sputtered indium tin oxide/indium phosphide solar cells has yet to produce a definitive model of the junction that takes account of all of the experimental evidence. The work here reports on a two-layer structure which was originally developed to avoid the surface degradation of bare InP that occurs under high-temperature processing conditions, but was found also to assist in the elucidation of some of the mechanisms, particularly the role of hydrogen and phosphorus movement, involved in ITO/InP cell performance. This two-layer technique effected marked improvements in output properties, which have previously been reported, and now we outline proposed operating mechanisms based on these results and on the work of other researchers in the area.

1. Introduction

The broad research effort dedicated to sputtered indium tin oxide/indium phosphide devices has not, so far, produced a single model of the junction, in particular its formation and operation, that takes account of all of the information from various experimentalists. At present there is some debate regarding the actual junction structure, of which the homojunction is the most popularly supported, but even more critical is the mechanism by which this is actually formed, whether by sputtering damage, Sn diffusion or phosphorus movement or by some other mechanism. The movement of phosphorus from InP substrates during sputtering and/or during back-contact formation plays a significant role in device performance. The work here reports on a unique two-layer structure which was developed to avoid the surface degradation of bare InP under high-temperature processing conditions such as those required for ohmic contact formation. The technique was shown to effect marked improvements in relative output properties, and coincidentally provided further insight into the nature of the junction. The conclusions about the junction appear to agree with those of other workers, who also prepared sputtered devices but who used different methods to prevent surface damage.

Our method of preventing this degradation was to sputter deposit a protective layer on the InP surface before potentially damaging heat processes such as back-contact sintering were carried out. A second layer was then deposited to complete the photovoltaic junction. This second layer acts as both a current-collecting layer and a junction-inducing layer. This resulted in markedly improved outputs compared to those of the single-layer devices, and these were further improved by post-deposition annealing treatments to the films.

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Our devices also showed behaviour put forward by other researchers, which supported mechanistic arguments concerning phosphorus movement under sputtering, sintering and annealing conditions.

In this paper, we will firstly report on the gains made from these double-layer photovoltaic structures of ITO/InP and secondly outline some proposed operating mechanisms based on our work and on that reported by other researchers. A comparison of our device output results with those of other workers is also made.

Table 1. Comparison of cells with annealed layers.

Cell	Features	Layer thickness (Å)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	J_{light} (mA cm^{-2})	J_{sc}/J_{light}	FF (%)	η (%)
1	Single layer		550	11.31	39.22	0.29	27.0	1.69
9	ITO ITO	337 461	623	33.61	39.21	0.86	51.0	12.39
21	In/Sn ITO	325 507	657	21.41	23.36	0.92	55.4	7.79
22	In/Sn ITO	191 613	683	32.37	36.47	0.89	52.7	11.66
23	In/Sn ITO	78 755	718	36.1	42.19	0.86	49.8	13.07
26	In/Sn Vacuum H_2 ITO Vacuum H_2	129 529	648	29.38	34.69	0.84	37.5	7.14
27	In/Sn ITO Vacuum H_2	72 854	678	44.00	47.1	0.93	55.1	16.46
28	In/Sn Vacuum H_2 ITO	80 706	662	32.86	42.61	0.77	19.7	4.28
29	In/Sn Vacuum Ar ITO Vacuum H_2	89 701	704	37.10	40.50	0.92	60.8	15.87
30	In/Sn Vacuum Ar ITO Vacuum Ar	69 697	638	33.86	35.92	0.94	52.7	11.37

2. Experimental detail

The zinc-doped p-InP substrates were obtained from Crystacomm, California. They were degreased and lightly etched prior to device fabrication [1]. Initially, the back contacts were evaporated onto the lapped side of substrates from Au–Zn (95%–5%) wire supplied by the Wilkinson Company, California. Next was the deposition of the first of two layers in this

structure. The purpose of the two-layer configuration was to minimize damage incurred on the bare front surface of the cell during the high-temperature stage which was required for ohmic back-contact formation and which was found to be degrading device performance [2]. InP has a low congruent temperature of 370 °C [3–5], so when it is exposed to high temperatures, irreversible degradation of the InP occurs. Prior FTIR studies had shown clearly that there were compositional changes to the InP surface when a bare substrate was heated at temperatures as low as 200 °C [6]. It has been shown that when InP is exposed to temperatures above the congruent temperature, a loss of P occurs producing non-stoichiometric surfaces which have an associated high density of dangling bonds and which in turn lead to poor devices.

The first layer, layer 1, was deposited by dc sputtering from a target of 90 wt% In_2O_3–10 wt% SnO_2 but the series resistance of the devices was high, due to the oxide nature of the material, producing poor device performance. The behaviour of these cells is typified by that of cell 9 listed in table 1. The series resistance was decreased by sputtering the first layer from a metal In–Sn target, 10 wt% In–90 wt% Sn in a hydrogen–argon mixture (about 20% hydrogen). The optimal thickness for this layer was found to be approximately 80 Å as shown in table 1 [2]. Since In–Sn is a metal, films generally have low-transmission properties and so very thin layers were needed to ensure reasonable light transmission while still obtaining low values of series resistance.

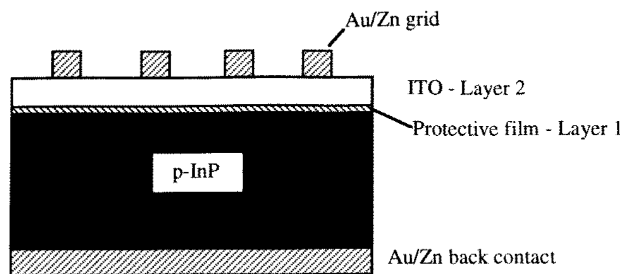

Figure 1. The structure of the cells.

The next important step was the formation of the ohmic contact to the back of the device by sintering. The devices were heated in a conventional open-tube furnace in argon at 380 °C for five minutes. Layer 2 was then sputtered from a target of 90 wt% In_2O_3–10 wt% SnO_2 in an argon ambient giving a thickness of ∼700 Å. After the deposition of each of these layers, some of the devices were left to cool overnight in a hydrogen-rich or argon atmosphere (about 10^{-1} mbar) in the vacuum chamber as detailed in table 1. Finally a rudimentary grid of Au–Zn was evaporated onto the front surface. The main thrust of our research work was to find optimal fabrication techniques involving layer thickness and materials while at the same time avoiding other procedures which could further damage the surface. It was therefore decided that an evaporated grid would suffice instead of the potentially damaging photolithographic processes. This adversely affects the fill factor, but overall improvements are still quite evident. It needs to be noted therefore that the reported devices are not of high efficiency but simply indicators of techniques bringing about improvement. All of the devices were tested under 100 mW cm^{-2} (1 Sun) illumination from a Schoeffel solar simulator with a spectral output closely similar to that of the AM1 spectrum. The structure of the devices is depicted in figure 1.

3. Results

The main results for our devices are summarized in table 1. A number of devices were fabricated using the same procedures and the best of each of these devices is listed in table 1 as representative of the behaviour of each set of cells. Where no atmosphere is listed, no annealing took place and the device was left to cool under vacuum until the next step was carried out.

The results for the best single-layer device produced in this work are included for comparison with those for the double-layer devices. The fabrication procedure of this device is the same as that for the double-layer devices except that no protective layer was deposited prior to ohmic contact sintering.

3.1. Single- and double-layer structures

It can be seen from the results in table 1 that a marked improvement in device performance was effected by depositing a protective layer before any heating steps took place.

3.2. ITO versus In–Sn for layer 1

Using In–Sn instead of ITO for the first layer markedly improved device performance even though the films were less optically transmissive due to the metallic nature of the In–Sn film.

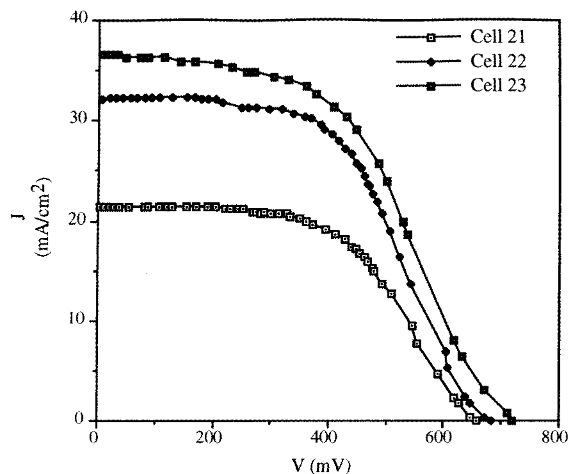

Figure 2. Light J–V characteristics of cells 21, 22, 23.

3.3. The thickness of layer 1

Cells 21, 22 and 23 were prepared to indicate an optimal thickness for layer 1 trading off series resistance and optical transmissivity. The generated current, J_{light}, increased with decreasing layer 1 thickness, due to greater transmissivity, but the proportion of collected current (the ratio of J_{sc} to J_{light}) decreases although the absolute collected current (J_{sc}) increased. From these, and other device results, it was determined that layer 1 should be of

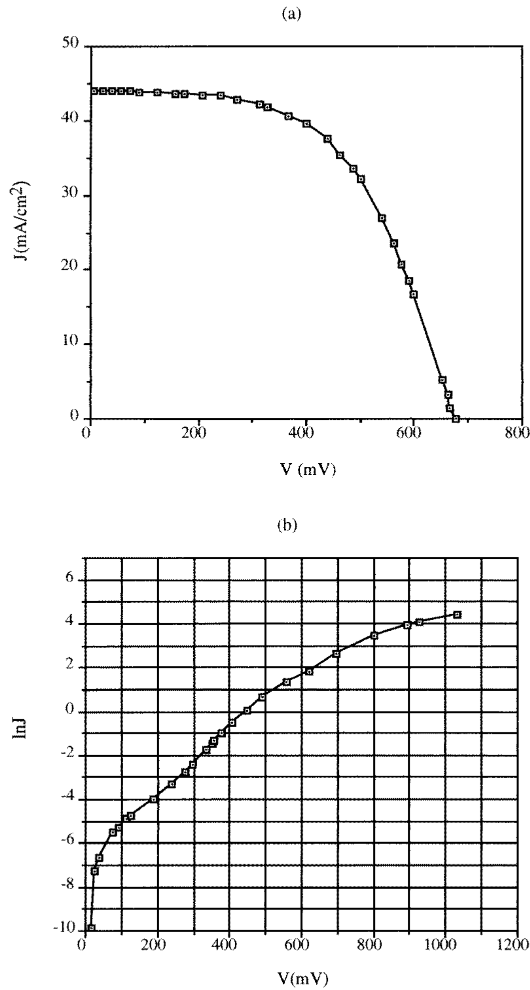

Figure 3. Output characteristics of cell 27: (a) the illuminated J–V characteristic; (b) the dark ln J–V characteristic.

the order of 80 Å. Figure 2 shows a comparison of the illuminated V–J characteristics of cells 21, 22 and 23.

3.4. In-chamber annealing effects

Sputtered films tend to have structural stresses associated with them, as the method of deposition is by means of high-energy particles bombarding the InP surface. Initially it was thought that in-chamber annealing each of the layers by cooling in hydrogen overnight might relieve some of the film stresses and also prevent any film oxidation. This, however, produced a worse device, cell 26, than a cell with no in-chamber annealing. At first it was not clear whether this was due to the annealing of layer 1 or the annealing of layer 2, which would have caused faster cooling of the device, or whether it was some interaction due to the hydrogen itself. This is discussed further in the discussion section. Cells 27 and 28 were used to clarify some of the possible mechanisms occurring. From these cells it could

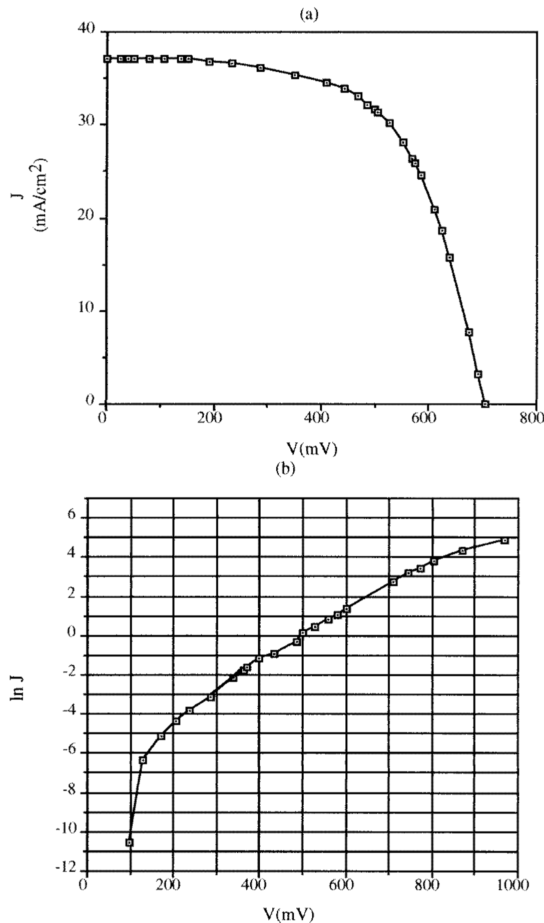

Figure 4. Output characteristics of cell 29: (a) the illuminated J–V characteristic; (b) the dark ln J–V characteristic.

be seen that it is vital that layer 1 is *not* annealed in hydrogen as indicated by cells 26 and 28. In fact, it is better not to anneal layer 1 at all (as was the case for cell 27) than to anneal it in hydrogen.

Comparing cells 27 and 29 where layer 2 has been annealed in hydrogen but layer 1 has either not been annealed at all (cell 27) or has been annealed in argon (cell 29), the fill factor is better for the argon-annealed cell but the actual efficiency is marginally better in cell 27. We consider that the good performance of cell 29 is a result of the optimal fabrication procedures; however, because layer 1 is thicker, its superiority is not obvious. The thicker layer 1 leads to a decreased light transmissivity evident from the lower current parameters whereas all other aspects are improved. The dark and illuminated V–J characteristics of cells 27 and 29 are shown in figures 3 and 4 respectively.

3.5. The effect of the thickness of layer 1 on $V_{diffusion}$

From measurements of the variation of the open-circuit voltage with temperature it was possible to determine the value of the diffusion voltage, $V_{\mathrm{diffusion}}$ (or the ideal built-in

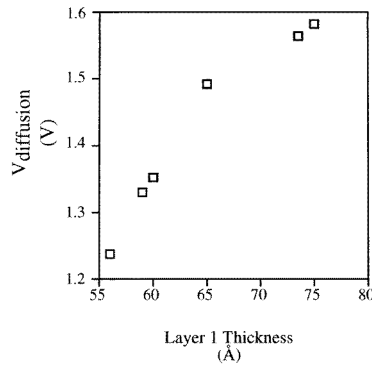

Figure 5. A plot showing $V_{\mathrm{diffusion}}$ versus the layer 1 thickness.

potential) which was obtained by plotting V_{oc} as a function of temperature. Since V_{oc} increases monotonically with decreasing temperature [7], the values of V_{oc} extrapolated to 0 K indicate the diffusion potential of the junction. An interesting relationship between the thickness of layer 1 and the diffusion voltage was found to exist and this is shown in figure 5. It is believed that layer 1 was partially oxidized during the back-contact sinter and so acts like an insulating layer which causes the diffusion voltage to change. This point is detailed further in the discussion section.

It should be noted that the results given in table 1 are based on gains made relative to the single-layer device first made and the clear improvements can be seen from this table. In this we have used net area or active area in order to take account of our rudimentary grid, i.e. we have taken the actual area covered by the sputtered films (total area) and subtracted from this the grid area. This is our definition of active area.

Table 2. Comparison of results from other workers and the results from cell 29 from this work.

Parameter	Cell 29	Tsai *et al* [7]	Coutts and Naseem [25]	Dhere *et al* [16]	Coutts *et al* [26]	Gessert *et al* [15]
V_{oc}	0.704 V	0.69	0.717	0.608	0.809	0.798
J_{sc}	21.4 mA cm^{-2}	23.4	29.2	26.313	25.5	28.48
FF	60.8%	65	54.6	75.1	83.1	82.9
η	9.48%	12.4	12.4	12	17.1	18.8

However, in order to make use of the mechanistic arguments proposed by other workers, we have reverted to using the total area in table 2, so we have an absolute comparison with their results and more importantly with their conclusions regarding the junctions and mechanisms.

Because we have taken a very conservative value for the device area and have not included the effects of our very poor grid, the results do not appear to be particularly noteworthy except insofar as they are reasonably comparable with those of the others. The similarity of the results is sufficient for it to be reasonable to assume that the effects of process variations in these cells can be referred to the results given by other workers. The cells listed in table 2 were all sputtered ITO/InP cells, with different methods used to prevent surface damage (such as chemical and sputter etching) from affecting device performance.

As well as the results shown in table 2, a comparison of the built-in voltage V_{bi} was also made. From measurements made by using the V_{oc} versus T method, Luo and Thomas [18] found $V_{\mathrm{diffusion}} = 1.1$ V while Tsai *et al* [7] found 1.25 V and our work showed $V_{\mathrm{diffusion}} = 1.501$ V. While this is a slightly higher result, we believe this to be due to a slight oxidation of layer 1 which has occurred during sintering of the back contact, as mentioned above. C–V measurements were not made by the authors, but both Luo and Thomas [18] and Tsai *et al* [7] found these values to be anomalously large.

Table 3. Some of the theories regarding the ITO/InP structure.

Structure	Supporting evidence
nip [5]	Spreading resistance showed that within the InP wafer there is 100 nm of low resistance, 250 nm of high resistance and then a value of resistance which would be expected for the bulk.
MIS [6]	C–V measurements indicated that there was a semi-insulating layer formed in the InP substrate due to the accumulation of Fe and Cr on the surface. Annealing causes a return to the virgin state and the semi-insulating layer decreases. Anodic oxides give the same C–V results as sputtered ITO. This work rules out tin diffusion and sputter damage as possible causes of the junction.
[7]	C–V profiling shows no change in carrier density within 0.1 μm of the junction for a spray pyrolysis device.
Heterojunction [8, 9]	The spectral response of a junction formed at low temperatures looks like that of a heterojunction. This could also indicate a semiconductor–insulator–semiconductor structure. High temperatures resulted in a buried homojunction.

4. Discussion

The operating mechanisms of ITO/InP cells are complex, with a number of theories proposed to try to explain the behaviours reported by many workers. Table 3 summarizes some of the proposed possible structures such as the heterojunction, MIS and nip structures and the results which have led to these conclusions, many of which are not universally accepted. Table 4 summarizes the main evidence that ITO/InP behaves as a homojunction (HJ) and possible causes of the junction formation. The structure favoured by us is that of a homojunction.

4.1. Sn diffusion

One of the earliest theories put forward to explain junction formation was that the diffusion of Sn from the ITO film into the front surface of InP caused type conversion. Bachmann *et al* [13] found that Sn does in fact diffuse into InP at 250 °C. The explanation for photovoltaic behaviour at temperatures below this, e.g. at room temperature, was that only a very shallow junction was formed at low temperatures and a deep junction was formed at 250 °C when tin diffusion was significant. This theory however appears to be contradicted by several experimentalists, as detailed below.

Table 4. Possible causes of homojunction (HJ) operation.

Mechanism	Reference	Notes
Sn diffusion	[10]	Diffusion of Sn into InP generating buried HJ. At 25 °C, no Sn diffusion → heterojunction; at 250 °C, significant diffusion → deep homojunction.
Thermal damage	[11]	Junction formation due to thermally induced damage from sputtering.
	[4]	Spectral response of a HJ. Sputtered tin-free oxides on InP and PV devices still obtained. Heat treatment eventually led to an inferior device whereas Sn diffusion should be enhanced and so improve device performance with heating. Oxide/InP with no sputter damage exhibits PV behaviour.
Sputter damage	[12]	Tin-free cells give PV cells. Therefore the cause is not tin diffusion but is perhaps sputter damage.
	[13]	Plasma exposure time increases, resulting in improved quantum efficiency.
	[14]	RBS showed displacement of In atoms from equilibrium positions after sputtering.
	[15]	In_2O_3 was deposited and the cells were essentially the same as that of ITO/InP → not tin diffusion. Plasma damage was induced but with no film deposition. Result: PV device, only the series resistance changed. Sputtered ITO layer removed and disorder found at the interface.
	[16]	No increase in barrier height of ITO/p-InP with heating. If heating had induced the junction then the junction should have improved.
	[19]	ITO/p-Si. Low power does not induce a junction in Si. Could mean that the ITO/InP junction forms due to the sensitive nature of InP.
Loss of P	[4]	Loss of P → vacancies → donors.
Defect generation	[16]	C–V measurements.
Hydrogenation	[13]	H_2 cells have better long-λ response and poorer short-λ response. Either (a) a deeper junction or (b) more surface damage. Higher V_{oc}.

(a) Tsai *et al* [7] sputtered the oxides In_2O_3, CdO, ZnO and SnO_2 onto InP substrates and it was found that all of these oxides produced photovoltaic junctions whether Sn was present or not. Experiments by Coutts *et al* [17] gave similar results.

(b) If tin diffusion was the cause of junction formation, then the junction should in fact improve with heating. Luo and Thomas [18] and other workers found that this was not the case.

4.2. Thermal and sputtering damage

It is probable that thermal damage and sputtering damage both lead to phosphorus loss as P has a high vapour pressure. P preferentially depletes from the surface of InP under argon bombardment [4] and this could therefore lead to P vacancies which may be the principal

donors forming the n-type layer on damaged InP. Other, more complex, defects could also be present [7, 18].

Tsai *et al* [7] thought it likely that the damage-induced n layer would change with heating as the damage should 'anneal out'. They believed that this could be due to one of three effects or a combination of these:

(i) out-diffusion of defects;

(ii) formation of larger voids, i.e. a lower donor density resulting from the combining of these voids;

(iii) the in-diffusion of Zn acceptors (from p-type InP). If loss of P is the cause of junction formation then it would appear that heating should enhance the loss of P and therefore the junction should improve rather than anneal back to a p-type one.

As regards our own work, we think that the junction is caused by movement of P from the InP lattice, rather than loss of P to the atmosphere. Movement of P occurs when P shifts from its equilibrium position in the lattice to a non-equilibrium position. Loss of P occurs at temperatures above 300 °C and movement of P occurs at temperatures below this as shown in our own and other FTIR studies [1, 3]. In terms of the junction, movement of P and loss of P will result in the same thing, i.e. an n layer. However, loss of P, which occurs at a higher temperature, may also be associated with Zn in-diffusion, the out-diffusion of defects and/or the formation of larger voids due to higher temperatures, resulting in worse overall PV behaviour.

4.3. Mechanisms of phosphorus movement

The movement of phosphorus is of fundamental importance in the mechanisms of junction formation. From the evidence of many researchers it is thought that *movement* of P is sufficient to lead to a donor layer, which is preferable to *loss* of P which results in more gross effects on the substrate and hence poorer consequent devices [3, 7, 18, 20, 21].

Temperatures that are high enough induce phosphorus loss from the surface may also lead to other effects, such as *Zn migration* (which leads to an acceptor layer, i.e. a p-type one), *too much loss of P* (which leads to gross surface damage and hence large trap densities) and *annealing of defects* (the larger voids leading to a decreased defect density and hence reducing the density of the n layer) which may adversely affect photovoltaic behaviour. It is generally thought that there are three stages in the movement of P in InP; firstly it moves to the surface (diffusion), then it accumulates at the surface and finally P desorbs from the surface [20].

During ohmic contact formation in our single-layer devices, we believe that we had loss of P and therefore gross surface damage [1]. The photovoltaic behaviour was not due to a homojunction structure but from a heterojunction formed as a consequence of the deposition of the ITO layer (usually considered to be of n^+ type). Poor device performance resulted from material mismatches that are typical of heterojunctions and the gross surface damage caused by high-temperature contact formation.

Indications of a markedly different electronic structure were inferred when our two-layer devices showed greatly superior performances to those of the single-layer devices. We think that layer 1 acted as a blanket, both protecting the InP surface from gross surface damage and also acting as a 'collector' of phosphorus. Then, because P is not lost to the atmosphere, some of it can move back into the P-deficient surface of the substrate during the sputtering of layer 2. This movement would be due to the effects of bombarding the surface with particles and the normal wattage heating of the substrate during sputtering.

The surface trap density, initially caused by the movement of P into the In–Sn layer, will be partially passivated by the return of some of the P from the blanketing layer. It appears that the surface is however still left slightly deficient in P and thus acts as an optimal n layer giving a homojunction device.

4.4. Sputter etching and plasma exposure

Sputter etching is where the substrate is put in place of the target and bombarded by ions, thereby removing the surface and plasma exposure is when the substrate is placed in its usual position and exposed to an essentially non-depositing plasma which is usually at lower power than would be used in a normal run. Many workers use sputter etching to clean the surface of InP substrates and others have found that a low-power plasma exposure increases the quantum efficiency of InP cells. Pearsall [4] investigated the effects of sputter etching and plasma exposure on the InP surface. It was found that sputter etching resulted in gross physical changes resulting from the preferential etching of P from the surface. These samples showed strong photovoltaic behaviour. Plasma-exposed samples, on the other hand, showed no obvious surface modification as compared with the unexposed samples. Thermal studies were also carried out [4] and effects similar to those found in plasma exposure (no obvious surface modification) resulted, implying that plasma exposure damage is probably thermal in origin. The photovoltaic activity in these samples was found to be slight, and gentle rubbing of the surface could eliminate the effect. This plasma exposure was carried out for two to three minutes which was sufficient to induce photovoltaic behaviour [4] but perhaps not long enough to effect a permanent photovoltaic behaviour. Coutts *et al* [3, 11] compared the performance of devices which had had substrates exposed to a low-power plasma for between 0 and 60 minutes. It was found that the quantum efficiency of devices improved with increased exposure time. Devices which had had plasma exposure were far superior in efficiency to those with no exposure. It is believed that little gross surface damage resulted, but some movement of P may have occurred, also perhaps the low-power plasma exposure resulted in superior devices because of the removal of any native oxides which may have been present. This ties in with our belief that loss of P and movement of P both give an n layer, but loss of P causes more gross changes.

4.5. I–V and C–V results

The structure favoured by the authors is that of a homojunction and this is supported by the work of Luo and Thomas [18]. They sputter deposited ITO on n-InP and p-InP substrates and then for comparison evaporated Au on n-InP and on p-InP after which C–V and I–V measurements were taken and studied. They showed that ITO deposited on InP generates an n (or more probably an n^+) layer on the substrate surface as follows:

(i) p-InP: a raised barrier and donor-like defects implies there is an n^+ layer present;
(ii) n-InP: lowered barriers and ohmic behaviour, which again implies an n^+ layer.

This was considered sufficient evidence to conclude that no insulating layer is formed and so the proposed metal–semi-insulating–semiconductor (M–SI–S) and MIS structures were not valid and the ITO/InP structure is that of a homojunction. C–V measurements were also taken and anomalously high values of $V_{\mathrm{diffusion}}$ were found [22].

Some of the results from our own work indicate that the large values of $V_{\mathrm{diffusion}}$ obtained from C–V measurements made by other workers may in fact be due to the presence of an oxide layer. A clear relationship between the thickness of layer 1 and the diffusion voltage

was found as shown in figure 5. This led us to speculate that there probably is an insulating layer present, though its role in photovoltaic behaviour has not yet been fully determined, but it probably provides a secondary mechanism for the dominant homojunction behaviour rather than a classical MIS structure. It is possible that layer 1 was oxidized during back-contact formation, leading to this insulating layer [22].

4.6. The role of hydrogen in junction formation

Workers [21] who fabricated devices using a hydrogen ambient to sputter a 5 nm layer of ITO and then an oxygen-rich ambient to sputter a 50 nm layer of ITO produced some excellent devices. The higher V_{oc} which was obtained was thought to be due to one or a combination of the following factors.

(a) Hydrogen causes an increase in the doping density and hence the built-in potential and consequently V_{oc}. The mechanism for this could be that hydrogen cleans the surface of native oxide and removes traces of unstable oxides and so enhances the effects of energetic particle bombardment to cause an increase in the emitter doping density, assuming that movement of P is the cause of junction formation.

(b) Hydrogen neutralizes the shallow donors and shallow acceptors [15]. H^+ can also act as a donor [23], so an n layer is formed and the overall result is that the emitter doping density is increased. The net gain would clearly be more effective in a p-type than in an n-type material.

(c) The reduction of the saturation current density, J_0, is explained in terms of surface recombination. Analysis showed that recombination at the type-converted layer was negligible [21].

The poor short-wavelength response is explained by the fact that the junction depth was found to increase from 0.3 to 2 μm as the sputtering gas became increasingly rich with hydrogen [21]. Short-wavelength photons produce electron–hole pairs very close to where they are absorbed (i.e. at the InP surface) and so if the junction is very deep then the electron–hole pairs are likely to recombine before they reach the junction to be collected. As post-deposition heat treatment takes place, the junction moves toward the InP surface [21]. Since hydrogenation makes the junction deeper and heating makes the junction more shallow, heating must remove the effects of hydrogenation. This is in accordance with the results obtained in this work but not reported here. It was observed that the diffusion voltage and hence doping density decreased with heating. As most of the junction width lies across the lightly doped region, one can envisage the junction moving toward the surface as the emitter doping decreases. The movement of the junction would be caused by heating enhancing the return of P from the layer 1 In–Sn blanket and the return of P would be aided by the presence of H_2 during the in-chamber annealing of layer 1. It is thought that H_2 provides a lower energetic pathway for this return. At the point where P is going back to its original position the device structure would be essentially that of a heterojunction, that is n^+-ITO/p-InP instead of n^+-ITO/n-InP/p-InP. The previously dominating effect of the type-converted layer is weak and instead the ITO film is acting as an n-type layer. As a heterojunction, however, the device would exhibit poor output properties, as the lattice mismatch between the materials would be very large. InP has a lattice constant of 5.869 Å, while that of In_2O_3 is 10.118 Å and that of SnO_2 is 3.804 Å [24], all of which would indicate the existence of a large density of interface states. The transformation of ITO/InP from a homojunction to a heterojunction is supported by measurements of the spectral response before and after annealing [3]. Although the quantum efficiency improves, the actual device performance

does not, which is believed to be due to the increased number of recombination states caused by the above-mentioned lattice mismatch. Tsai *et al* [7] found that heat treatment of the junction caused the C–V data of an ITO/InP configuration to approach more closely those for a heterojunction. The devices fabricated in this programme, after sintering, have been found to have improved photogenerated current but not collected current, supporting the thesis of a heterojunction and an associated improved spectral response.

4.7. The presence of hydrogen during film deposition

The use of hydrogen during the fabrication of in-chamber-annealed devices has varying effects depending on the stage at which hydrogen is used. Hydrogen used in the sputter deposition of the In–Sn film, layer 1, acted merely to produce a metallic, and more conductive, film.

4.8. The presence of hydrogen during in-chamber annealing

Devices which were in-chamber annealed had varying degrees of success depending on when annealing took place. By far the most detrimental hydrogen anneal took place after the deposition of layer 1 (cell 26 and cell 28). As discussed previously, we believe that hydrogen assists the migration of P back into the InP substrate thereby producing a poorer junction. It is believed that the hydrogen provided a catalytic effect in forming an energetically favourable path for the phosphorus to move back into the InP, so the subsequent sintering step (to form the ohmic contact) puts more P back into the InP than would have otherwise occurred.

Once P had been assisted back into the InP by the anneal, a subsequent sputter deposition of layer 2 will still induce some damage (due to layer 1 being very thin) and a photovoltaic effect associated with this damage will still be observed. The photovoltaic effect seen in this cell would have been greater if layer 1 had been annealed in argon (or not at all) because less phosphorus would have moved back into the InP during the annealing process.

Hydrogen annealing after layer 2 deposition merely acts to reduce the resistance of the film, probably by reducing some of the oxygen content of the material. Since the ITO layer is quite thick, it is unlikely that the hydrogen could diffuse through this layer to affect the surface of the InP.

We believe that slow cooling of InP (such as would occur in cooling an InP substrate after film deposition in a vacuum) results in more time for the P from the bulk to partially neutralize the induced n layer, and hence the doping density would be reduced. A poorer junction would be produced. If, however, the InP is cooled in a gaseous environment (i.e. in-chamber annealing of InP), then cooling would be faster and so allow less time for P to move from the bulk to the induced n layer, and so be less effective in neutralizing the induced n layer. This would lead to a better junction. Other workers confirm that the movement of P depends strongly on the rate of cooling. Massies and Lemaire-Dezaly [20] found that rapid quenching of InP leads to a phosphorus-enriched surface and that slow cooling of InP results in a lower concentration of P at the surface, supporting our notion that fast cooling produces better junctions.

5. Conclusions

The general features of the model proposed to describe the ITO/InP devices in this work are listed below.

(1) The junction is formed by movement of P during sputtering (due to a combination of high-energy particles and thermal effects).

(2) Phosphorus is not actually lost to the environment but is collected in the In/Sn layer which has been sputtered on.

(3) Sintering forces P back into the InP substrate. Sintering InP at high temperatures with no protective layers causes permanent loss of P which aids junction formation but also causes very gross surface damage, with the result that the number of recombination traps increases and poor device performance results.

(4) Hydrogen has two roles in device performance:

(a) when used in the sputtering gas it acts to reduce oxides in In/Sn giving more conductive films; and

(b) when used to anneal layer 1 it enhances the movement of P back into InP, and with the subsequent sinter for back-contact formation more P (compared to the case for devices not subject to in-chamber annealing) goes into the InP substrate resulting in a poorer junction.

(5) Heat treatment eventually results in a heterojunction.

In terms of device fabrication procedures, marked gains have been made by using a combination of annealing steps incorporated into a double-layer-structure ITO/InP solar cell. From the results, it was found that in-chamber annealing of the sputter-deposited layers markedly improved device performance. The gases in which these layers were annealed play a vital role in junction mechanisms. The optimal devices were fabricated by following the procedure used to fabricate cell 29, i.e. having layer 1 annealed in argon and layer 2 in hydrogen.

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